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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,365	12/12/2003	Chaur-Chin Yang	BHT-3183-63	8705

7590 02/25/2005

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/733,365	YANG ET AL.
	Examiner	Art Unit
	Nimesh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *4 and 12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of Embodiment I, claims 1-3 and 5-11 in Paper No. 2 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US Pat. 5903052) in view of Paniccia (US Pat. 5895972).

Regarding claims 1-3, 5 and 6, Chen et al. disclose a BGA type/conventional thin-type BGA semiconductor package (see 10 in Fig. 1) comprising:

- a composite multilayered substrate (CMLS)/printed wiring board substrate (PWBS) including a MLS/PWB (see 24/12a/12b in Fig. 1) and a heat spreader/heat slug (HS-16 in Fig. 1),
- wherein the MLS/PWB having an upper surface, a lower surface and an opening (see 26/12e in Fig. 1), the opening passes through the upper surface and the lower surface, a step is formed in the opening (see Fig. 1)

- a plurality of ball pads (36/34 in Fig. 1) are formed on the lower surface, a plurality of bonding sites/connecting pads are formed on the step (not numerically referenced in Fig. 1; see bonding wire connections on the surface 12a in Fig. 1; Col. 4, lines 14-20) and electrically connect with the ball pads
- the HS being attached to the lower surface of the MLS/PWB and covers the opening to form a chip cavity
- an integrated circuit (IC) chip (14 in Fig. 1) disposed in the chip cavity, the chip having an active/upper surface and a back/lower surface
- a plurality of bonding pads being formed on the active surface and electrically connected to the connecting pads of the wiring board (see Fig. 1), the back surface of the chip being attached to the HS
- a package body comprising an encapsulate/dispensing material/sealant (30 in Fig. 1) being formed in the chip cavity of the composite substrate sealing the IC chip and bonding wires (see 30, 14 and 20 respectively in Fig. 1)
- a plurality of solder bumps/balls (22 in Fig. 1) on the ball pads
- the HS having a thickness being smaller than the height/diameter of the solder bumps/balls (see Fig. 1 and 5)
- the HS having an exposed lower surface opposing the surface being attached to the MLS/PWB, a solder/metal (see 44 at the lower surface of 16 in the final structure of Fig. 5; Col. 4, lines 30-46) film being formed on the exposed surface

(Fig. 1-5; Col. 2, line 45- Col. 4, line 46)

Chen et al. disclose the HS being attached to the back/lower surfaces of the chip and the MLS/PWB, but fail to teach using a dummy die being attached to those lower surfaces.

Paniccia teaches a thermally dissipative wire bonded package having a heat slug (HS) being attached to a back surface of a device/chip (see 820 and 802 respectively in Fig. 9A) wherein the HS comprises a dummy substrate without any electrical connections therein, such as dummy silicon die substrate (820 in Fig. 9A) to provide the desired thermal performance for the device application requirement (Col. 8, lines 1-20; Col. 5, lines 57-63).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a dummy die being attached to the lower surfaces of the chip and the wiring board as taught by Paniccia so that the desired thermal dissipation can be achieved in Chen et al's BGA.

Regarding claim 7, Chen et al. and Paniccia teach the entire claimed structure as applied to claim 5 above, wherein Chen et al. further teach using a conventional adhesive/bonding material such as epoxy/thermosetting compound to provide adhesion/mechanical bonding among the substrates including the HS, MLS/PWB and the chip (Col. 3, line 5 and lines 35-38).

Regarding claims 8-11, Chen et al. and Paniccia teach the entire claimed structure as applied to claims 1-3 above, wherein Chen et al. further teach:

- the HS including a central region and a peripheral region surrounding the central region, the peripheral region being attached to the lower surface of the MLS/PWB
- the back surface of the IC chip being attached to the central region of the HS

(see Fig. 1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

02-21-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800